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High Speed and Energy Efficient Carry Skip Adder

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Abstract— In this paper a novel carry skip adder structure of 32 bit has been proposed that have better speed and less power consumption than the conventionally used. In this we are analysing the delay, area and power consumption of currently available different carry skip structures, firstly analyse conventional carry skip structure, then we modified the structure for better performance by using the concatenation and incrementation scheme. Then analyze the hybrid variable latency carry skip adder by replacing the nucleus stage of concatenation and incrementation scheme with parallel prefix adder. Later we uses different CSKA implementations in convolver for performing a convolution function along with 16 x 16 reversible Vedic multiplier and the delay and energy consumption of each one is studied. Verilog HDL is used for designing the circuits and Xilinx software tool is used for estimating the delay and power consumption.

Keywords— Carry Skip Adder , Convolver, Delay, Hybrid Variable Latency, Skip technique ,UrdhvaTiryakbhyam sutra, , VHDL.

INTRODUCTION

Adders are digital circuit that executes addition of numbers. In numerous computers and other types of processors adders are used in the arithmetic logic units or ALU. They are also applied in other parts of the processor, where they are used to compute addresses, table indices, increment and decrement operators, and similar operations. Adders are a key building block in arithmetic and logic units (ALUs) and hence increasing their speed and reducing their power/energy consumption strongly affect the speed and power consumption of processors. There are many works on the subject of optimizing the speed and power of these units. Obviously, it is highly desirable to achieve higher speeds at low-power/energy consumptions, which is a challenge for the designers of general purpose processors. One of the effective techniques to lower the power consumption of digital circuits is to reduce the supply voltage due to quadratic dependence of the switching energy on the voltage. There are different types of adders are available according to our demands. They are normally two types of adders: binary adders and multiple bit adders. Carry skip adders are multiple bit adders which is also known as a carry-bypass adder. It is a skip the logic in propagation of carry and its operation is to speed up the additional operation and to adding the propagation of carry bit around portion of complete adder where it is an adder implementation that increases on the delay of a ripple-carry adder with little effort related to other adders. The enhancement of the worst-case delay is attained by using several carry-skip adders to form a block-carry-skip adder. In this paper we estimates delay and power consumption of different carry skip adders using these adders in convolver for performing the convolution function in digital signal processing. There are different adder families are available for estimation of delay and power including Ripple Carry Adder (RCA), Carry Select Adder(CSLA),Carry Skip Adder(CSKA) etc. From these CSKA is more efficient in case of delay and power consumption.

The CSKA consist of chain of Full Adders(FAs), RCA and 2:1 multiplexer. These multiplexers are used to connect RCAs.The delay of CSKA is depends on number of Fas .There are many methods are suggested for determining optimum delay .It uses the VSS (variable stage size) to minimize the delay. In [17] proposes new technique to reduce the optimal path delay. There are some methods are proposed to improve performance of adder at low voltage levels. It examines the CLSA better performance. Finally uses the hybrid structure to improve the efficiency and speed of adder.

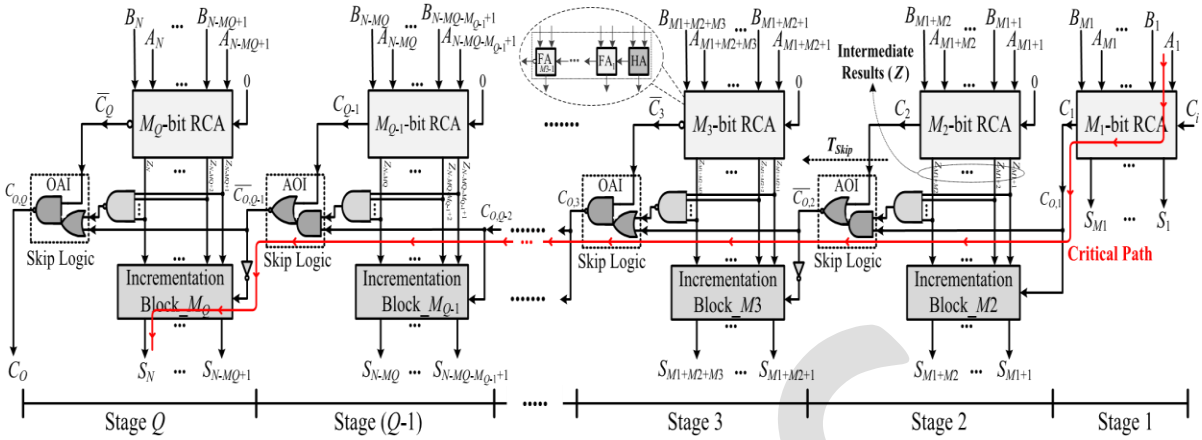

Fig 1: Structure of CI CSKA

CONVENTIONAL CARRY SKIP ADDER

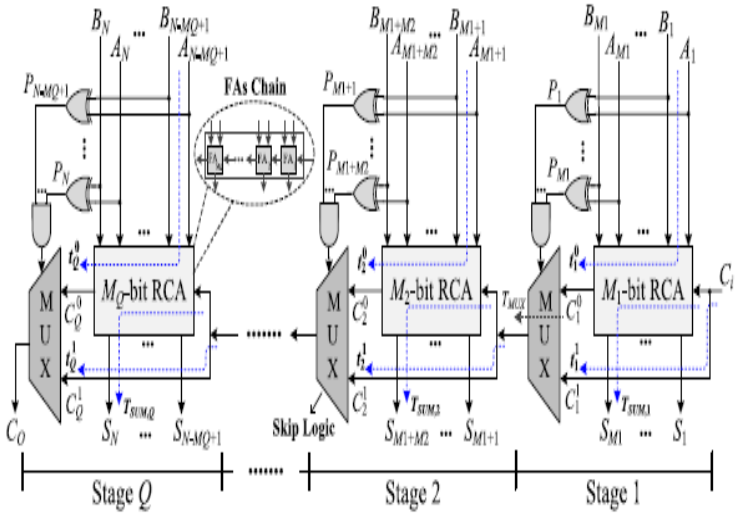

Fig 2: Conventional CSKA

The structure of conventional carry skip adder is shown in fig 2,which is based on blocks of RCAs.In addition to RCA blocks ,there is chain of FAs in each stage and skip logic using 2:1 multiplexer. In the CSKA, the carry skip logic detects the situation, and makes the carry ready for the next stage without waiting for the operation of the FA chain to be completed. The skip operation is performed using the gates and the multiplexer shown in the figure 1.The CSKA can be implemented by VSS and FSS .Where VSS CSKA is more efficient.

A. Fixed Stage Size CSKA

In this CSKA, assumes that each stage of CSKA contains M FAs ,then for N bit CSKA there is Q number of stages i.e Q =M/N ,where Q is an integer. The critical path of CSKA consists of FA chain of first stage, multiplexer on intermediate stage and FA chain on last stage.

B. Variable Stage Size CSKA

Thus using the variable sizes to each stage we can increase the speed which is shown in fig 3.It is achieved by lowering the delays of first and third terms in fig 1.These delays are minimized by lowering the size of first and last RCA blocks.

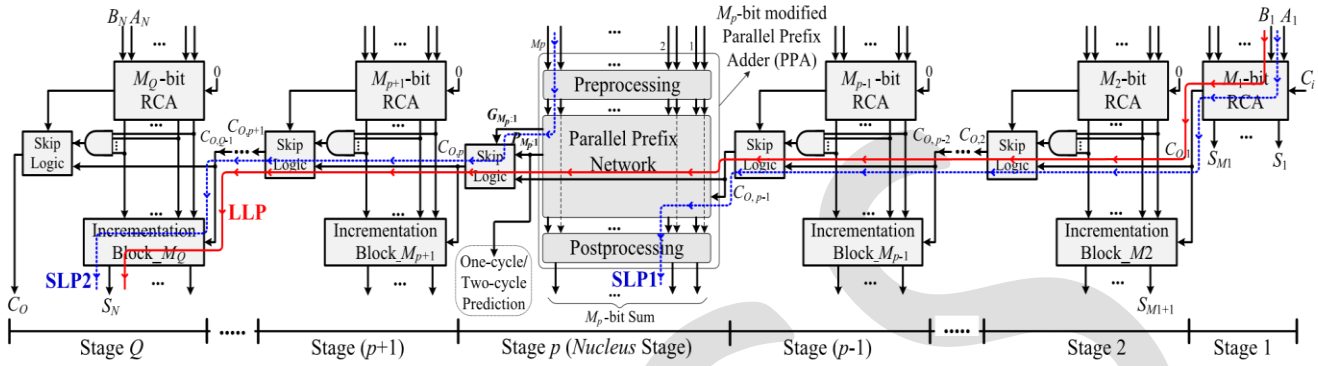

Fig. 3.Structure of hybrid variable latency CSKA

V.HYBRID VARIABLE LATENCY CSKA

Hybrid variable latency adder structure is similar to CI CSKA structure which is shown in fig 3.For making the hybrid variable latency structure to CSKA ,we have to replace some of the middle stages of CI CSKA with PPA(parallel prefix adder).This structure has higher speed than conventional one. The figure 5 shows the hybrid variable latency structure. In this structure we are using parallel prefix network of brent kung adder [4] is used .One of the advantages of using this PPA is that it uses forward paths ,so longest carry is calculated faster than others anf fan out is also lesser than other ones.The PPA has used in nucleus stage of CI CSKA .It has three levels of operation ,first the preprocessing level where propagate signals and generate signal for inputs are calculated.In the next level we are using brent kung adder parallel prefix network to calculate all intermediate signals.Finally in postprocessing stage final summation is calculated which is shown in fig 4.

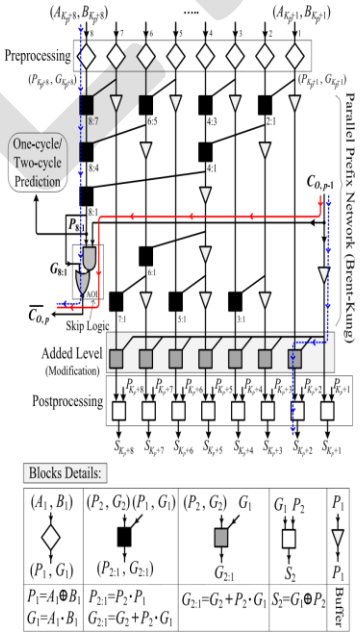

Fig 4. Internal structure of hybrid variable latency CSKA.

Convolution is assumed to be the necessary operation used in most of the signal processing applications. Convolution is a mathematical operation executed on two functions, producing a third function that is typically observed as an efficiently modified version of one of the two original functions. It is used for different applications comprising probability, statistics, computer vision, language processing, image and signal processing, engineering, and differential equations. So it is very important to develop a technique which improves the speed of convolution operation.

Vedic mathematics is traditional mathematical form used by Aryans. It increases the speed of operation, and the algorithms are based on mind calculations. The calculations are based on 16 sutras, of which UrdhvaTiryakbhyam sutra is used for Vedic multiplication. The proposed design uses reversible logic, therefore the power dissipation and delay reduces greatly. In this paper, the delay, area and power of existing design is compared with proposed design.

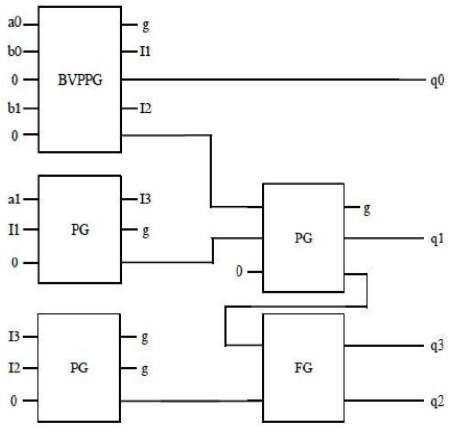

Fig 5: Reversible 2x2 UrdhvaTiryakbhyam multiplier

PROPOSED DESIGN

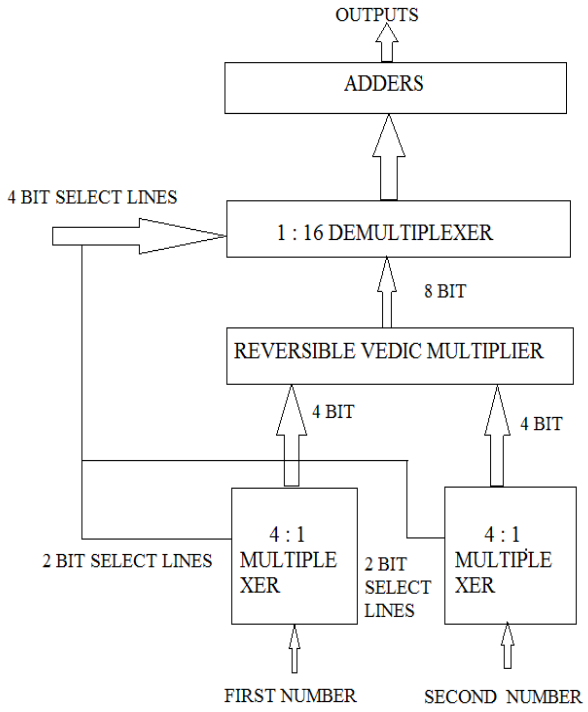

Fig 6. Block Diagram of Convolver

The convolution of two 4-bit numbers is calculated and realised using reversible logic. The multiplier and multiplicand are selected using two 4:1 multiplexers. Then the multiplication operation, that is, the Vedic multiplication is performed and is stored using 1:16 demultiplexer. The first two bit of four bit select line of demultiplexer is the select line of first 4:1 multiplexer. And the last two bits are the select line of second 4:1 multiplexer. Then the corresponding products are added in the adder section. The block diagram of the proposed design is shown in Figure 6. For the addition of two numbers carry look skip adder is selected.

RESULTS AND DISCUSSION

Simulation results obtained from Xilinx ISE design suite is observed and compare the delay and power consumption of different CSKAs.By analysing different CSKAs its evident that hybrid variable latency adder has lesser delay compared to other ones.But area is larger for this CSKA .

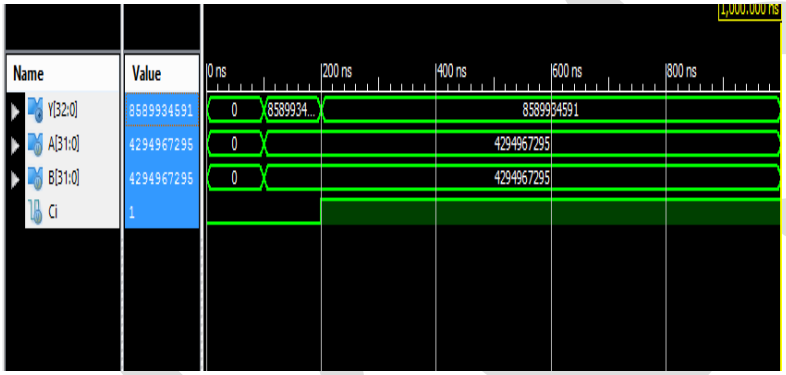

Fig 7. Simulation Result of CSKA

From the simulation results of different CSKAs,itscler that Conv CSKA occupies less space but delay is higher. In CI CSKA delay is less than CONV CSKA,butno.of LUTs used is higher than conventional one. In Hybrid Variable Latency CSKA also the delay is further reduced but no.of LUTs increased.

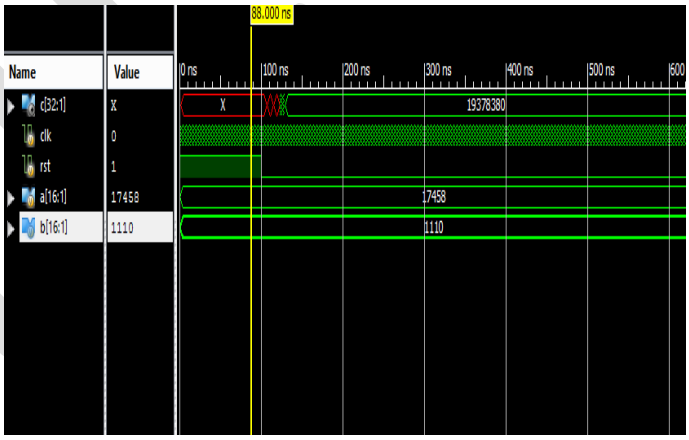

Fig 8. Simulation of Convolution using CSKAs.

Power dissipation is calculated using Xilinx Xpower Analyzer Tool. Energy consumption is product of delay and power dissipation and is tabulated in table 1.

Table 1. Comparison of various CSKA

ADDER DESIGN	NO.OF LUTS	DELAY(ns)	ENERGY(nJ)
CONV - CSKA	49	21.089	1.82
CI - CSKA	75	20.234	1.56
HYBRID CSKA	67	18.170	1.04

CONCLUSION

In this paper, different CSKA structures are analyzed using XILINX software and there delays and energy consumption are estimated. Then for better analyses we are using a convolver for performing convolution function ,where we are using different CSKA structures in convolver. From the analyses it's clear that Hybrid variable latency adder has higher speed and power consumption is also less. But area is larger than other ones.

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